Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**SOURCE**

**GATE**

**.084”**

**.103”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: G = .019” X .024”**

**Backside Potential: Drain**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .084” X .103” DATE: 5/3/22**

**MFG: INT’L RECTIFIER THICKNESS .014” P/N: IRFC9034N**

**DG 10.1.2**

#### Rev B, 7/19/02